DE0-CV Board

SCHEMATIC	*CONTENT*	*PAGE*
Cover	Cover Page	01
Block Diagram	Block Diagram	02
FPGA	FPGA IO, Clock, Configuration and Power	03 ~ 09
Memory	SDRAM, SD Card	10
Video	VGA	11
User Interface	GPIO_0,GPIO_1 - two 2x20 Header	12~13
User Interface	LED and 7'Segment	14
User Interface	PS2 and Switch and Key	15
Power	Power	16

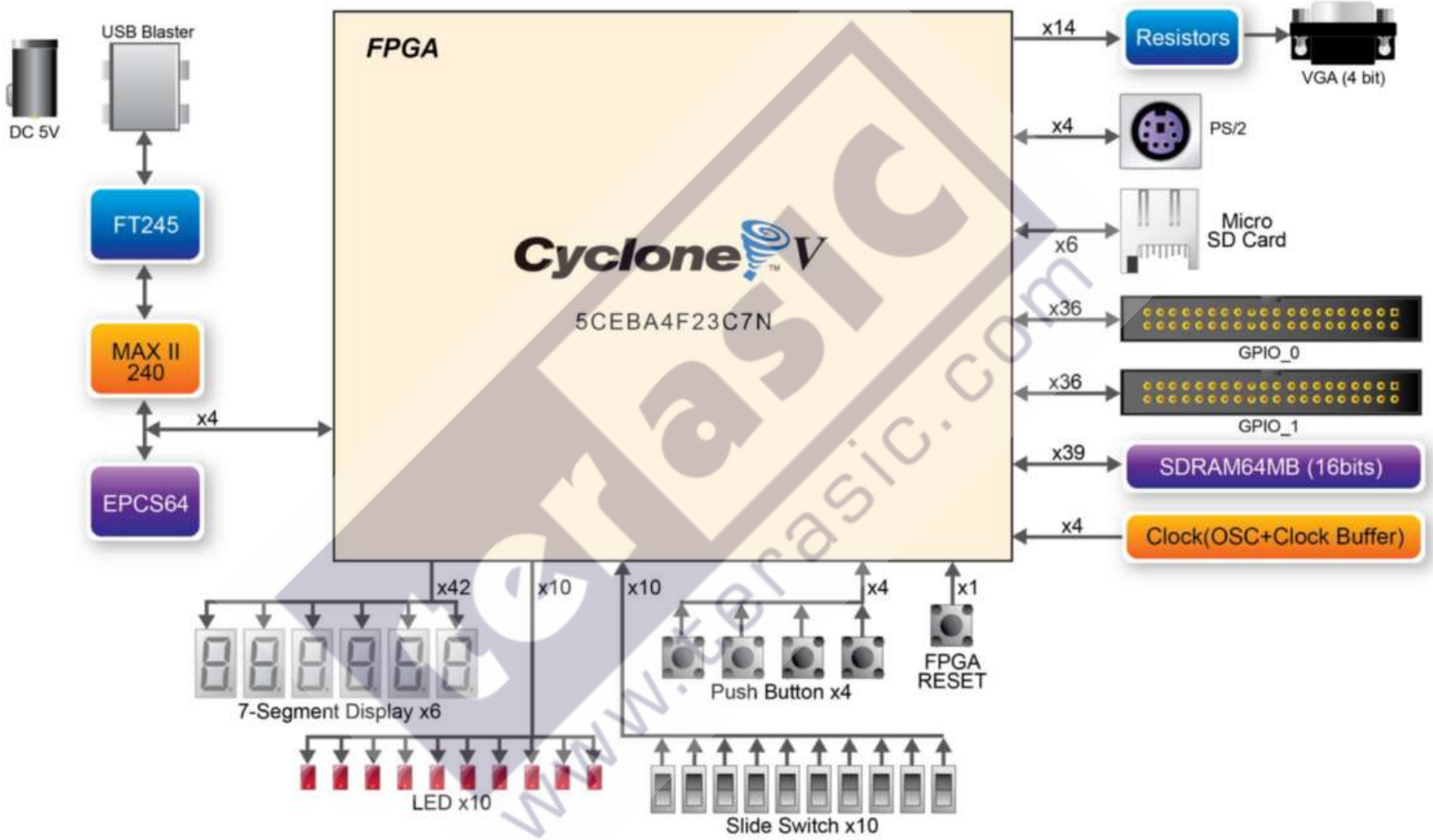
terasic
www.terasic.com

Copyright (c) 2011 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title
DE0-CV Board

Size	Document Number	Rev
B	Cover Page	C

Date: Wednesday, June 03, 2015 Sheet 1 of 17

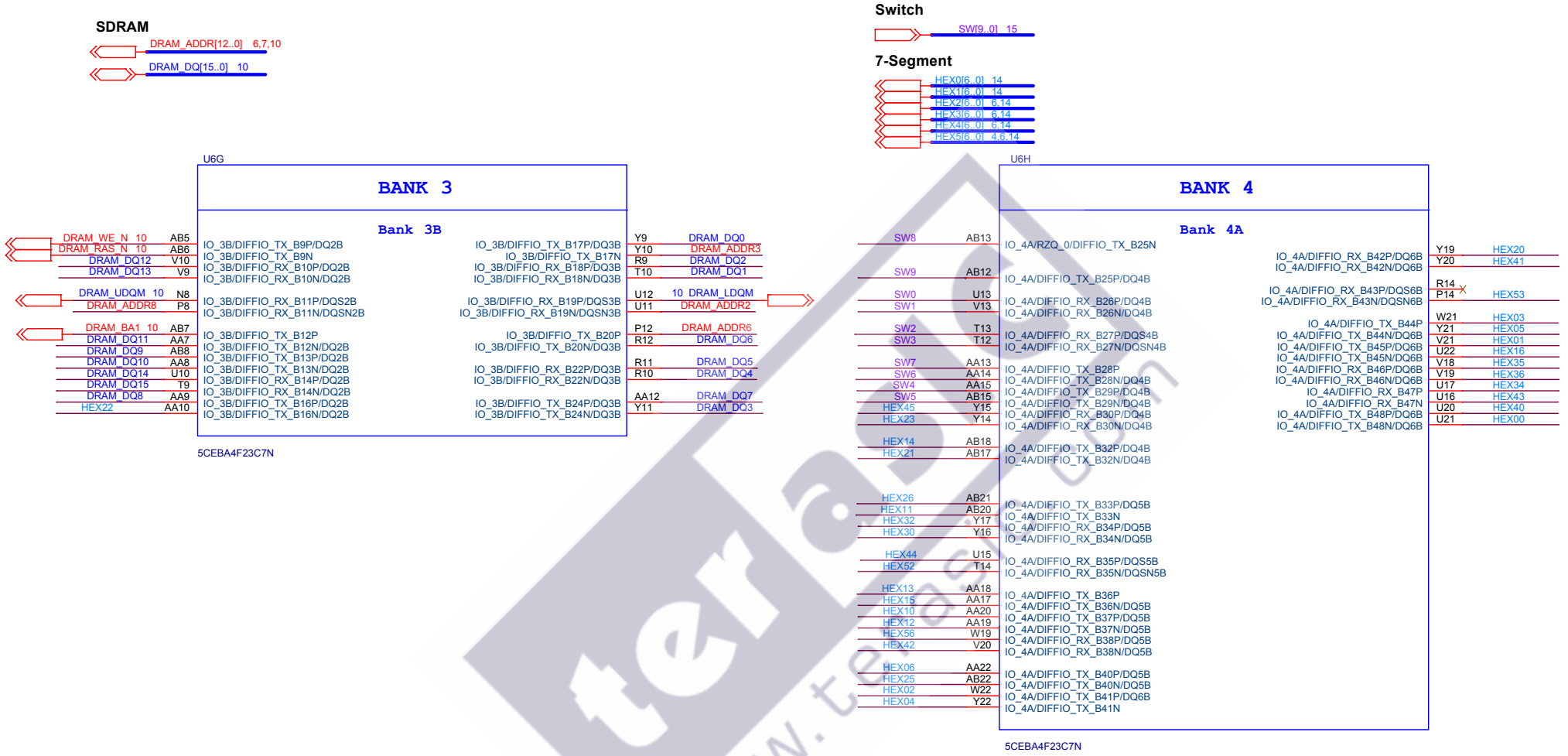


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title
DE0-CV Board

Size	Document Number	Rev
B	Block Diagram	C

Date: Wednesday, June 03, 2015 Sheet 2 of 17


SDRAM
DRAM_ADDR[12..0] 6,7,10
DRAM_DQ[15..0] 10
Switch
SW[9..0] 15
7-Segment
HEX0[6..0] 14
HEX1[6..0] 14
HEX2[6..0] 6,14
HEX3[6..0] 6,14
HEX4[6..0] 6,14
HEX5[6..0] 4,6,14
U6G
BANK 3
Bank 3B
DRAM_WE_N 10 AB5 IO_3B/DIFFIO_TX_B9P/DQ2B
DRAM_RAS_N 10 AB6 IO_3B/DIFFIO_TX_B9N
DRAM_DQ12 V10 IO_3B/DIFFIO_RX_B10P/DQ2B
DRAM_DQ13 V9 IO_3B/DIFFIO_RX_B10N/DQ2B
DRAM_UDQM 10 N8 IO_3B/DIFFIO_RX_B11P/DQS2B
DRAM_ADDR8 P8 IO_3B/DIFFIO_RX_B11N/DQSN2B
DRAM_BA1 10 AB7 IO_3B/DIFFIO_TX_B12P
DRAM_DQ11 AA7 IO_3B/DIFFIO_TX_B12N/DQ2B
DRAM_DQ9 AB8 IO_3B/DIFFIO_TX_B13P/DQ2B
DRAM_DQ10 AA8 IO_3B/DIFFIO_TX_B13N/DQ2B
DRAM_DQ14 U10 IO_3B/DIFFIO_RX_B14P/DQ2B
DRAM_DQ15 T9 IO_3B/DIFFIO_RX_B14N/DQ2B
DRAM_DQ8 AA9 IO_3B/DIFFIO_TX_B16P/DQ2B
HEX22 AA10 IO_3B/DIFFIO_TX_B16N/DQ2B
IO_3B/DIFFIO_TX_B17P/DQ3B Y9 DRAM_DQ0
IO_3B/DIFFIO_TX_B17N Y10 DRAM_ADDR3
IO_3B/DIFFIO_RX_B18P/DQ3B R9 DRAM_DQ2
IO_3B/DIFFIO_RX_B18N/DQ3B T10 DRAM_DQ1
IO_3B/DIFFIO_RX_B19P/DQS3B U12 10 DRAM_LDQM
IO_3B/DIFFIO_RX_B19N/DQSN3B U11 DRAM_ADDR2
IO_3B/DIFFIO_TX_B20P P12 DRAM_ADDR6
IO_3B/DIFFIO_TX_B20N/DQ3B R12 DRAM_DQ6
IO_3B/DIFFIO_RX_B22P/DQ3B R11 DRAM_DQ5
IO_3B/DIFFIO_RX_B22N/DQ3B R10 DRAM_DQ4
IO_3B/DIFFIO_TX_B24P/DQ3B AA12 DRAM_DQ7
IO_3B/DIFFIO_TX_B24N/DQ3B Y11 DRAM_DQ3
5CEBA4F23C7N
U6H
BANK 4
Bank 4A
SW8 AB13 IO_4A/RZQ_0/DIFFIO_TX_B25N
SW9 AB12 IO_4A/DIFFIO_TX_B25P/DQ4B
SW0 U13 IO_4A/DIFFIO_RX_B26P/DQ4B
SW1 V13 IO_4A/DIFFIO_RX_B26N/DQ4B
SW2 T13 IO_4A/DIFFIO_RX_B27P/DQS4B
SW3 T12 IO_4A/DIFFIO_RX_B27N/DQSN4B
SW7 AA13 IO_4A/DIFFIO_TX_B28P
SW6 AA14 IO_4A/DIFFIO_TX_B28N/DQ4B
SW4 AA15 IO_4A/DIFFIO_TX_B29P/DQ4B
SW5 AB15 IO_4A/DIFFIO_TX_B29N/DQ4B
HEX45 Y15 IO_4A/DIFFIO_RX_B30P/DQ4B
HEX23 Y14 IO_4A/DIFFIO_RX_B30N/DQ4B
HEX14 AB18 IO_4A/DIFFIO_TX_B32P/DQ4B
HEX21 AB17 IO_4A/DIFFIO_TX_B32N/DQ4B
HEX26 AB21 IO_4A/DIFFIO_TX_B33P/DQ5B
HEX11 AB20 IO_4A/DIFFIO_TX_B33N
HEX32 Y17 IO_4A/DIFFIO_RX_B34P/DQ5B
HEX30 Y16 IO_4A/DIFFIO_RX_B34N/DQ5B
HEX44 U15 IO_4A/DIFFIO_RX_B35P/DQS5B
HEX52 T14 IO_4A/DIFFIO_RX_B35N/DQSN5B
HEX13 AA18 IO_4A/DIFFIO_TX_B36P
HEX15 AA17 IO_4A/DIFFIO_TX_B36N/DQ5B
HEX10 AA20 IO_4A/DIFFIO_TX_B37P/DQ5B
HEX12 AA19 IO_4A/DIFFIO_TX_B37N/DQ5B
HEX56 W19 IO_4A/DIFFIO_RX_B38P/DQ5B
HEX42 V20 IO_4A/DIFFIO_RX_B38N/DQ5B
HEX06 AA22 IO_4A/DIFFIO_TX_B40P/DQ5B
HEX25 AB22 IO_4A/DIFFIO_TX_B40N/DQ5B
HEX02 W22 IO_4A/DIFFIO_TX_B41P/DQ6B
HEX04 Y22 IO_4A/DIFFIO_TX_B41N
IO_4A/DIFFIO_RX_B42P/DQ6B Y19 HEX20
IO_4A/DIFFIO_RX_B42N/DQ6B Y20 HEX41
IO_4A/DIFFIO_RX_B43P/DQS6B R14
IO_4A/DIFFIO_RX_B43N/DQSN6B P14 HEX53
IO_4A/DIFFIO_TX_B44P W21 HEX03
IO_4A/DIFFIO_TX_B44N/DQ6B Y21 HEX05
IO_4A/DIFFIO_TX_B45P/DQ6B V21 HEX01
IO_4A/DIFFIO_TX_B45N/DQ6B U22 HEX16
IO_4A/DIFFIO_RX_B46P/DQ6B V18 HEX35
IO_4A/DIFFIO_RX_B46N/DQ6B V19 HEX36
IO_4A/DIFFIO_RX_B47P U17 HEX34
IO_4A/DIFFIO_RX_B47N U16 HEX43
IO_4A/DIFFIO_TX_B48P/DQ6B U20 HEX40
IO_4A/DIFFIO_TX_B48N/DQ6B U21 HEX00
5CEBA4F23C7N
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.
Title
DE0-CV Board
Size B
Document Number
FPGA BANK 3, BANK 4
Rev C
Date: Wednesday, June 03, 2015
Sheet 3 of 17

LED

LEDR[9..0] 14

7-Segment

HEX5[6..0] 3,6,14

GPIO 0

GPIO_0[35..0] 5,6,7,12

U6L

BANK 2

Bank 2A

HEX55	C2	IO_2A/DIFFIO_TX_L9P/DQ1L	IO_2A/DIFFIO_TX_L13P/DQ1L	N2	LEDR4
HEX54	C1	IO_2A/DIFFIO_TX_L9N	IO_2A/DIFFIO_TX_L13N/DQ1L	N1	LEDR5
PS2_DAT_15	G2	IO_2A/DIFFIO_RX_L10P/DQ1L	IO_2A/DIFFIO_RX_L14P/DQ1L	U2	LEDR6
PS2_DAT2_15	G1	IO_2A/DIFFIO_RX_L10N/DQ1L	IO_2A/DIFFIO_RX_L14N/DQ1L	U1	LEDR7
			IO_2A/DIFFIO_RX_L15P	Y3	LEDR3
PS2_CLK_15	D3	IO_2A/DIFFIO_RX_L11P/DQS1L	IO_2A/DIFFIO_RX_L15N	W2	LEDR2
PS2_CLK2_15	E2	IO_2A/DIFFIO_RX_L11N/DQSN1L	IO_2A/DIFFIO_TX_L16P/DQ1L	AA2	LEDR0
			IO_2A/DIFFIO_TX_L16N/DQ1L	AA1	LEDR1
LEDR8	L2	IO_2A/DIFFIO_TX_L12P			
LEDR9	L1	IO_2A/DIFFIO_TX_L12N/DQ1L			

5CEBA4F23C7N

U6I

BANK 5

Bank 5A

GPIO_032	T19	IO_5A/RZQ_1/DIFFIO_TX_R1P/DQ1R
GPIO_035	T15	IO_5A/DIFFIO_RX_R4P/DQ1R
GPIO_028	R15	IO_5A/DIFFIO_RX_R4N/DQ1R
GPIO_030	R16	IO_5A/DIFFIO_RX_R6P/DQS1R
GPIO_029	R17	IO_5A/DIFFIO_RX_R6N/DQSN1R
GPIO_017	P19	IO_5A/DIFFIO_TX_R7P/DQ1R
GPIO_027	P18	IO_5A/DIFFIO_TX_R7N
GPIO_020	P16	IO_5A/DIFFIO_RX_R8P/DQ1R
GPIO_019	P17	IO_5A/DIFFIO_RX_R8N/DQ1R

Bank 5B

IO_5B/DIFFIO_TX_R10P/DQ2R	N20	GPIO_014
IO_5B/DIFFIO_TX_R10N/DQ2R	N21	GPIO_010
IO_5B/DIFFIO_RX_R11P/DQ2R	N19	GPIO_015
IO_5B/DIFFIO_RX_R11N/DQ2R	M18	GPIO_021
IO_5B/DIFFIO_RX_R13P/DQS2R	K17	GPIO_025
IO_5B/DIFFIO_RX_R13N/DQSN2R	L17	GPIO_023
IO_5B/DIFFIO_TX_R14P	M20	GPIO_08
IO_5B/DIFFIO_TX_R14N/DQ2R	M21	GPIO_09
IO_5B/DIFFIO_RX_R15P/DQ2R	L19	GPIO_024
IO_5B/DIFFIO_RX_R15N/DQ2R	L18	GPIO_022
IO_5B/DIFFIO_TX_R16P/DQ2R	K21	GPIO_06
IO_5B/DIFFIO_TX_R16N	K22	GPIO_07

5CEBA4F23C7N

Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title: **DE0-CV Board**

Size	Document Number	Rev
B	FPGA BANK 2, BANK 5	C

Date: Wednesday, June 03, 2015 Sheet 4 of 17



Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title: **DE0-CV Board**

Size	Document Number	Rev
B	FPGA BANK 7, BANK 8	C

Date: Wednesday, June 03, 2015 Sheet 5 of 17

SDRAM

DRAM_ADDR[12..0] 3,7,10

GPIO 0

GPIO_0[35..0] 4,5,7,12

GPIO 1

GPIO_1[35..0] 5,13

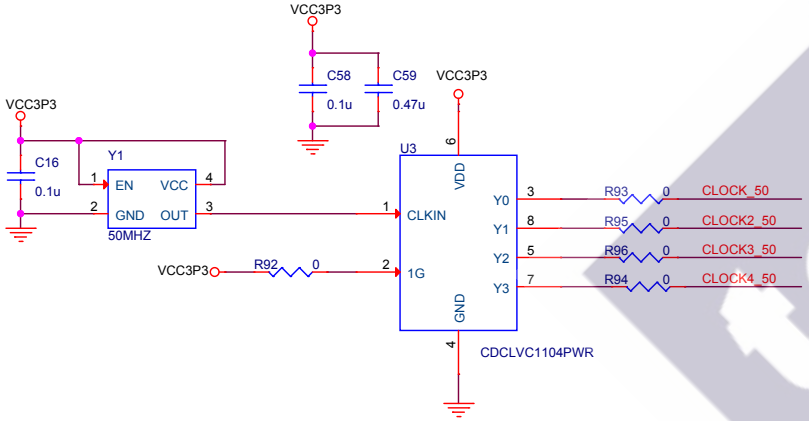
7-Segment

HEX2[6..0] 3,14

HEX3[6..0] 3,14

HEX4[6..0] 3,14

HEX5[6..0] 3,4,14



U6B

Clocks

Bank 3B

CLOCK_50 M9 IO_3B/CLK0P,FPLL_BL_FBP/DIFFIO_RX_B15P IO_3B/FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTP,FPLL_BL_FB/DIFFIO_TX_B21P/DQ3B → AB11 10_DRAM_CLK

HEX51 M8 IO_3B/CLK0N,FPLL_BL_FBN/DIFFIO_RX_B15N IO_3B/FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTN/DIFFIO_TX_B21N/DQ3B → AB10 DRAM_ADDR5

HEX50 N9 IO_3B/CLK1P/DIFFIO_RX_B23P

HEX46 P9 IO_3B/CLK1N/DIFFIO_RX_B23N

Bank 4A

CLOCK4_50 V15 IO_4A/CLK2P/DIFFIO_RX_B31P

HEX24 V14 IO_4A/CLK2N/DIFFIO_RX_B31N

HEX31 W16 IO_4A/CLK3P/DIFFIO_RX_B39P

HEX33 V16 IO_4A/CLK3N/DIFFIO_RX_B39N

Bank 5B

Clock_in GPIO_00 N16 IO_5B/CLK6P/DIFFIO_RX_R9P IO_5B/FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTP,FPLL_BR_FB/DIFFIO_TX_R12P/DQ2R → M22 GPIO_016 Clock_out

Clock_in GPIO_02 M16 IO_5B/CLK6N/DIFFIO_RX_R9N IO_5B/FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTN/DIFFIO_TX_R12N/DQ2R → L22 GPIO_018 Clock_out

Bank 7A

CLOCK2_50 H13 IO_7A/CLK10P/DIFFIO_RX_T17P

GPIO_132 G13 IO_7A/CLK10N/DIFFIO_RX_T17N

Clock_in GPIO_10 H16 IO_7A/CLK11P/DIFFIO_RX_T9P

Clock_in GPIO_12 H15 IO_7A/CLK11N/DIFFIO_RX_T9N

Bank 8A

CLOCK3_50 E10 IO_8A/CLK8P,FPLL_TL_FBP/DIFFIO_RX_T33P IO_8A/FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTP,FPLL_TL_FB/DIFFIO_TX_T28P/DQ4T → H8 11_VGA_HS

F9 IO_8A/CLK8N,FPLL_TL_FBN/DIFFIO_RX_T33N IO_8A/FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTN/DIFFIO_TX_T28N/DQ4T → G8 11_VGA_VS

G10 IO_8A/CLK9P/DIFFIO_RX_T25P

F10 IO_8A/CLK9N/DIFFIO_RX_T25N

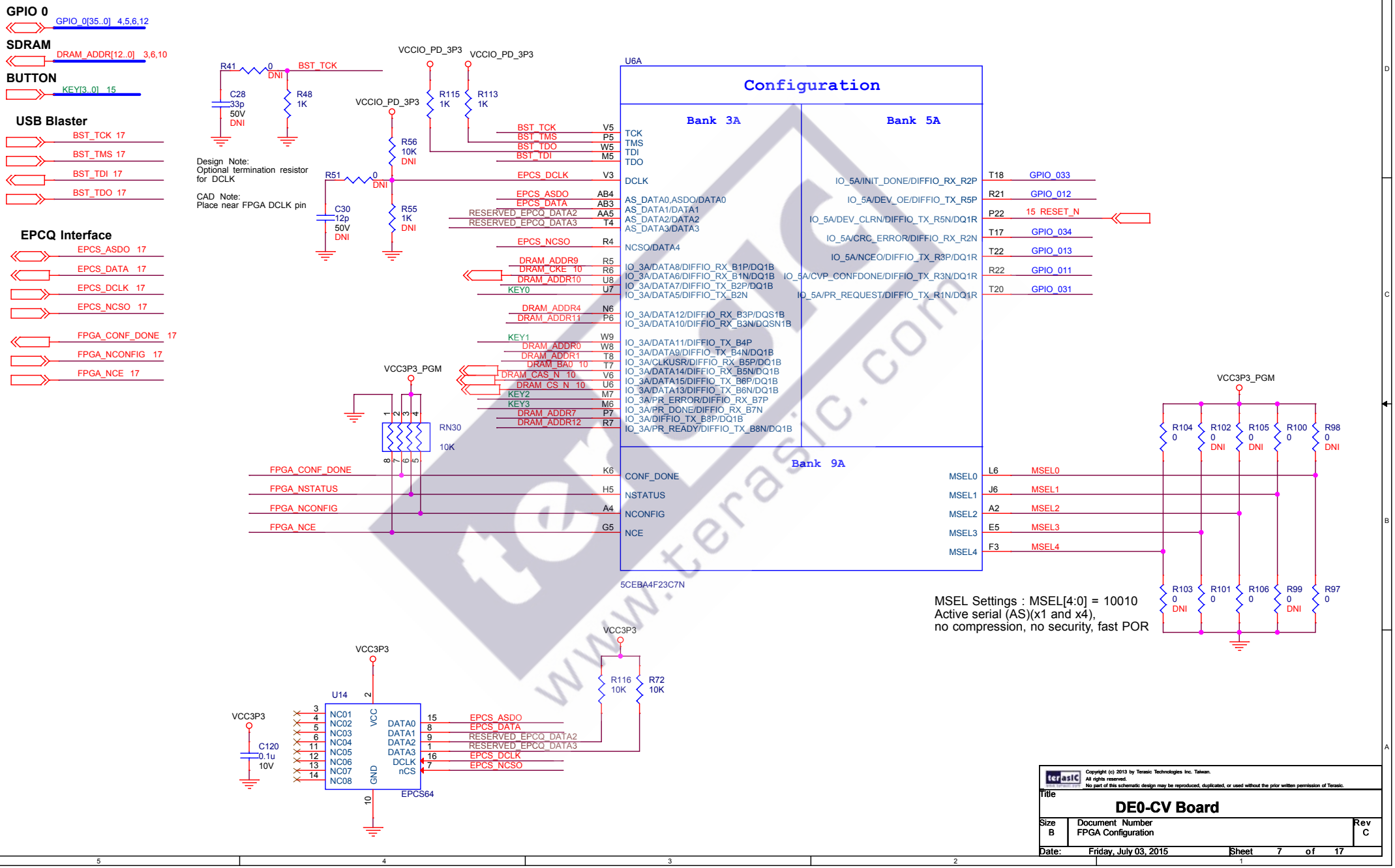
5CEBA4F23C7N

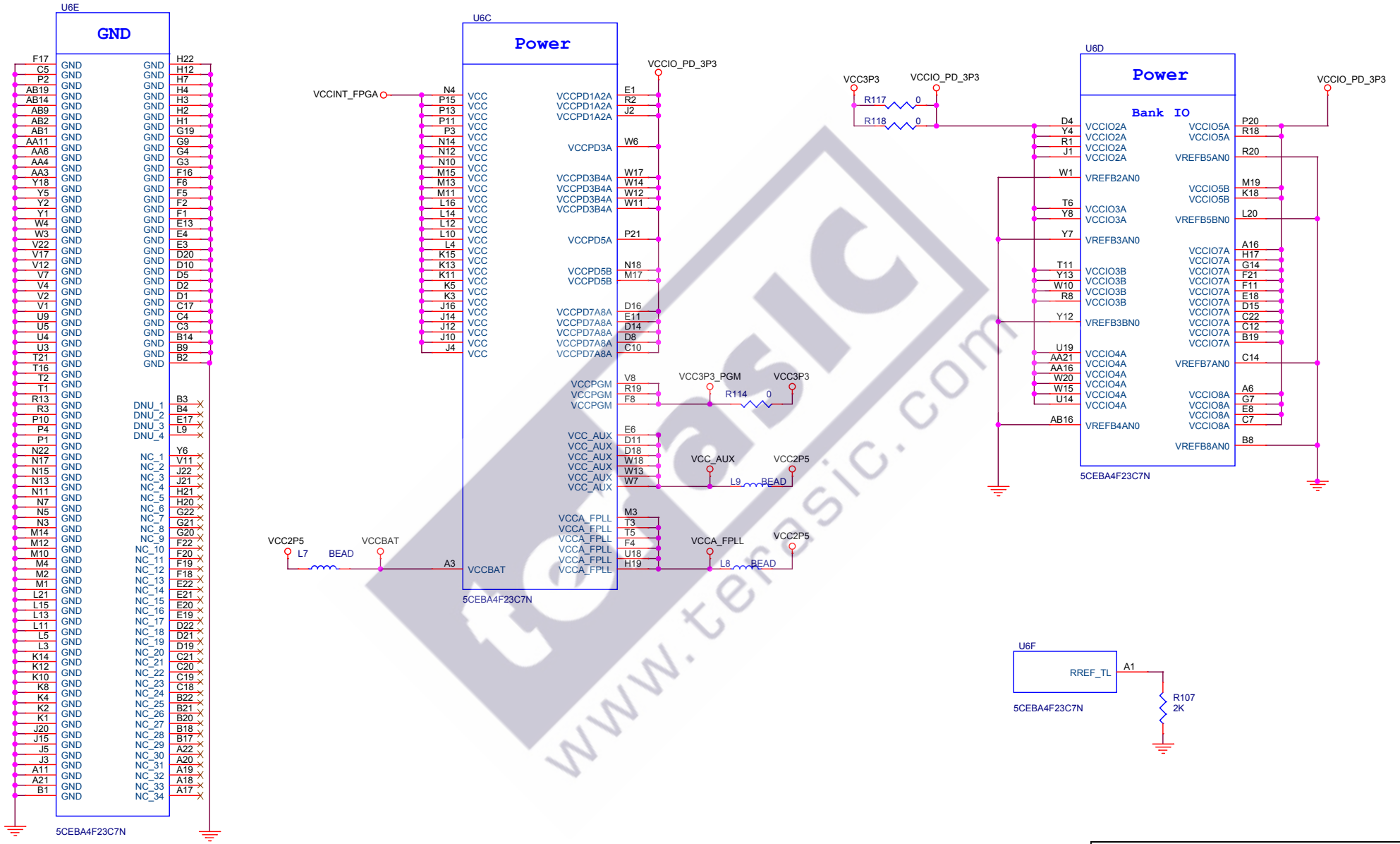
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title: **DE0-CV Board**

Size	Document Number	Rev
B	FPGA Clocks	C

Date: Friday, July 03, 2015 Sheet 6 of 17


GPIO 0
GPIO_0[35..0] 4,5,6,12
SDRAM
DRAM_ADDR[12..0] 3,6,10
BUTTON
KEY[3..0] 15
USB Blaster
BST_TCK 17
BST_TMS 17
BST_TDI 17
BST_TDO 17
EPCQ Interface
EPCS_ASDO 17
EPCS_DATA 17
EPCS_DCLK 17
EPCS_NCSO 17
FPGA_CONF_DONE 17
FPGA_NCONFIG 17
FPGA_NCE 17
R41 0 DNI
BST_TCK
C28 33p 50V DNI
R48 1K
VCCIO_PD_3P3
R115 1K
R113 1K
R56 10K DNI
R51 0 DNI
C30 12p 50V DNI
R55 1K DNI
Design Note:
Optional termination resistor for DCLK
CAD Note:
Place near FPGA DCLK pin
U6A
Configuration
Bank 3A
Bank 5A
Bank 9A
TCK
TMS
TDI
TDO
DCLK
AS_DATA0,ASDO/DATA0
AS_DATA1/DATA1
AS_DATA2/DATA2
AS_DATA3/DATA3
NCSO/DATA4
IO_3A/DATA8/DIFFIO_RX_B1P/DQ1B
IO_3A/DATA6/DIFFIO_RX_B1N/DQ1B
IO_3A/DATA7/DIFFIO_TX_B2P/DQ1B
IO_3A/DATA5/DIFFIO_TX_B2N
IO_3A/DATA12/DIFFIO_RX_B3P/DQS1B
IO_3A/DATA10/DIFFIO_RX_B3N/DQSN1B
IO_3A/DATA11/DIFFIO_TX_B4P
IO_3A/DATA9/DIFFIO_TX_B4N/DQ1B
IO_3A/CLKUSR/DIFFIO_RX_B5P/DQ1B
IO_3A/DATA14/DIFFIO_RX_B5N/DQ1B
IO_3A/DATA15/DIFFIO_TX_B6P/DQ1B
IO_3A/DATA13/DIFFIO_TX_B6N/DQ1B
IO_3A/PR_ERROR/DIFFIO_RX_B7P
IO_3A/PR_DONE/DIFFIO_RX_B7N
IO_3A/DIFFIO_TX_B8P/DQ1B
IO_3A/PR_READY/DIFFIO_TX_B8N/DQ1B
CONF_DONE
NSTATUS
NCONFIG
NCE
IO_5A/INIT_DONE/DIFFIO_RX_R2P
IO_5A/DEV_OE/DIFFIO_TX_R5P
IO_5A/DEV_CLRN/DIFFIO_TX_R5N/DQ1R
IO_5A/CRC_ERROR/DIFFIO_RX_R2N
IO_5A/NCEO/DIFFIO_TX_R3P/DQ1R
IO_5A/CVP_CONFDONE/DIFFIO_TX_R3N/DQ1R
IO_5A/PR_REQUEST/DIFFIO_TX_R1N/DQ1R
MSEL0
MSEL1
MSEL2
MSEL3
MSEL4
5CEBA4F23C7N
BST_TCK V5
BST_TMS P5
BST_TDO W5
BST_TDI M5
EPCS_DCLK V3
EPCS_ASDO AB4
EPCS_DATA AB3
RESERVED_EPCQ_DATA2 AA5
RESERVED_EPCQ_DATA3 T4
EPCS_NCSO R4
DRAM_ADDR9 R5
DRAM_CKE_10 R6
DRAM_ADDR10 U8
KEY0 U7
DRAM_ADDR4 N6
DRAM_ADDR11 P6
KEY1 W9
DRAM_ADDR0 W8
DRAM_ADDR1 T8
DRAM_BA0_10 T7
DRAM_CAS_N_10 V6
DRAM_CS_N_10 U6
KEY2 M7
KEY3 M6
DRAM_ADDR7 P7
DRAM_ADDR12 R7
T18 GPIO_033
R21 GPIO_012
P22 15_RESET_N
T17 GPIO_034
T22 GPIO_013
R22 GPIO_011
T20 GPIO_031
L6 MSEL0
J6 MSEL1
A2 MSEL2
E5 MSEL3
F3 MSEL4
VCC3P3_PGM
RN30
10K
FPGA_CONF_DONE K6
FPGA_NSTATUS H5
FPGA_NCONFIG A4
FPGA_NCE G5
R104 0
R102 0 DNI
R105 0 DNI
R100 0
R98 0 DNI
R103 0 DNI
R101 0
R106 0
R99 0 DNI
R97 0
MSEL Settings : MSEL[4:0] = 10010
Active serial (AS)(x1 and x4),
no compression, no security, fast POR
VCC3P3
R116 10K
R72 10K
U14
NC01
NC02
NC03
NC04
NC05
NC06
NC07
NC08
VCC
GND
DATA0
DATA1
DATA2
DATA3
DCLK
nCS
EPCS64
C120 0.1u 10V
EPCS_ASDO
EPCS_DATA
RESERVED_EPCQ_DATA2
RESERVED_EPCQ_DATA3
EPCS_DCLK
EPCS_NCSO
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.
Title
DE0-CV Board
Size B
Document Number
FPGA Configuration
Rev C
Date: Friday, July 03, 2015
Sheet 7 of 17



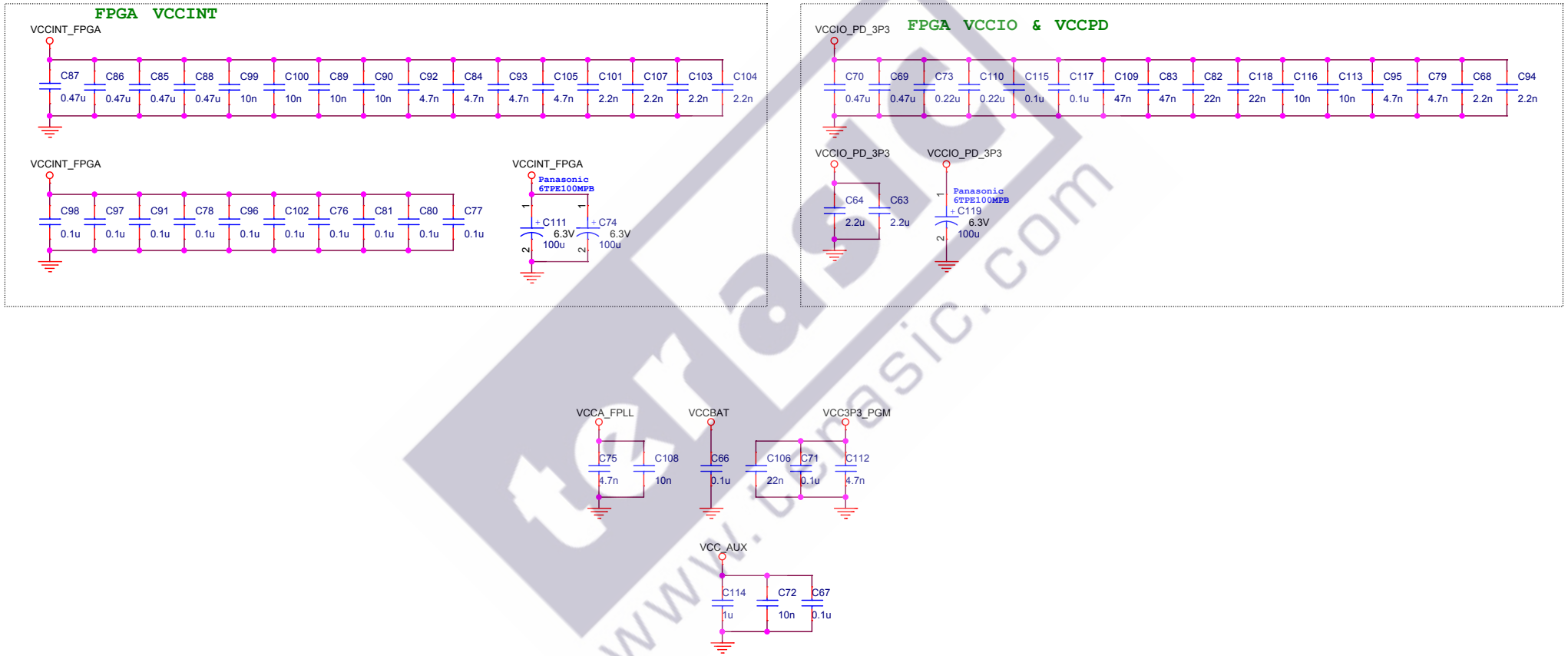
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title

DE0-CV Board

Size	Document Number	Rev
B	FPGA Power , GND	C

Date: Friday, July 03, 2015 Sheet 8 of 17



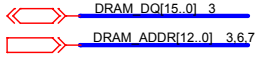
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

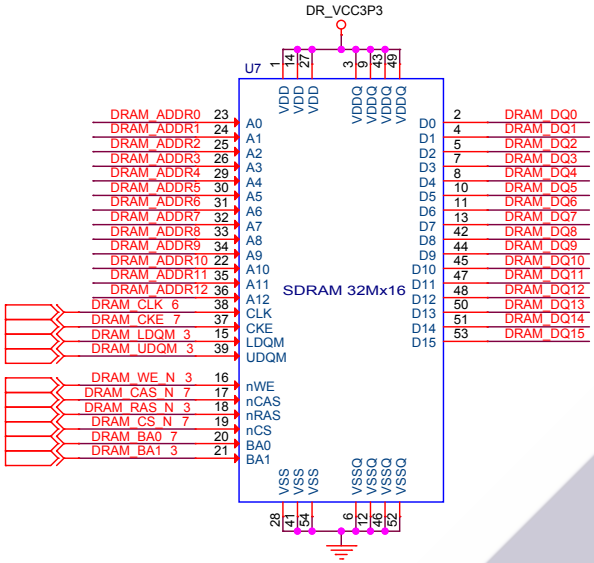
Title
DE0-CV Board

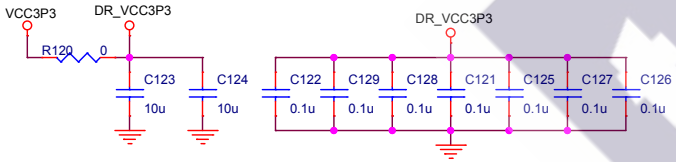
Size	Document Number	Rev
B	FPGA Decoupling	C

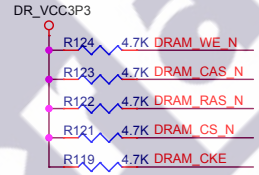
Date: Friday, July 03, 2015 Sheet 9 of 17

SDRAM

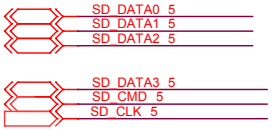


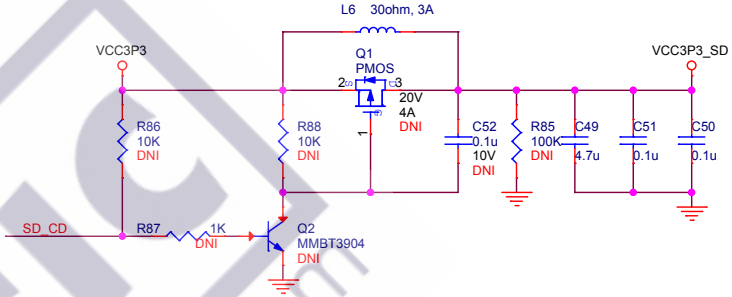


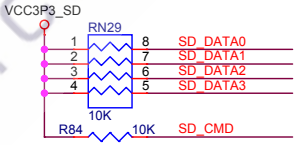


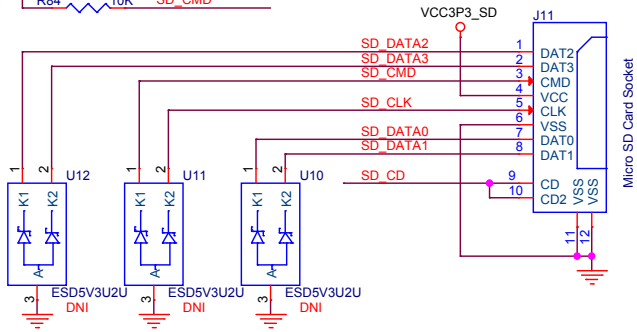


Micro SD Card









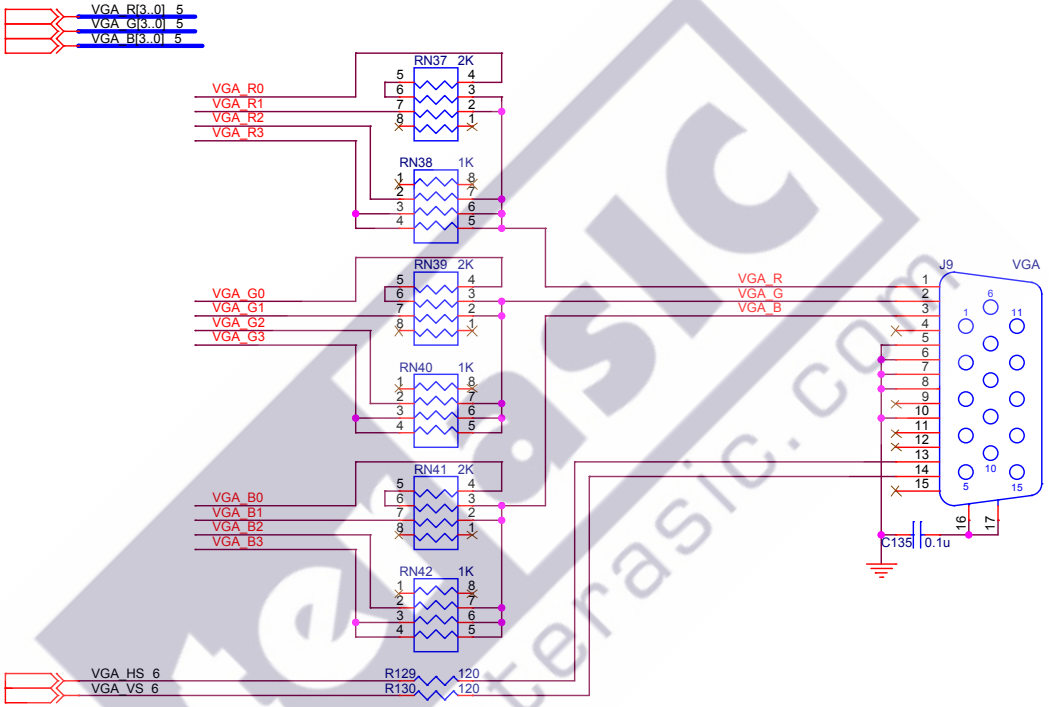
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title: **DE0-CV Board**

Size	Document Number	Rev
B	SDRAM , SD CARD	C

Date: Friday, July 03, 2015 Sheet 10 of 17

VGA



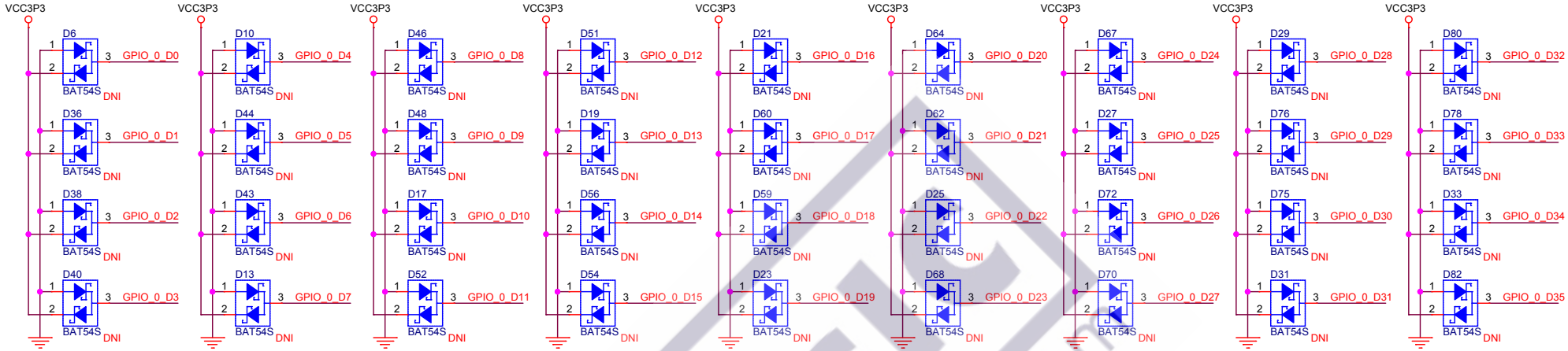
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title

DE0-CV Board

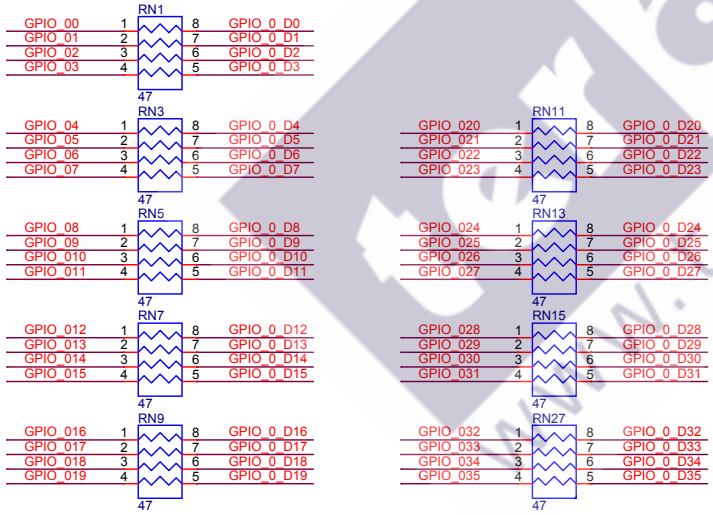
Size	Document Number	Rev
B	VGA	C

Date: Wednesday, June 03, 2015 Sheet 11 of 17

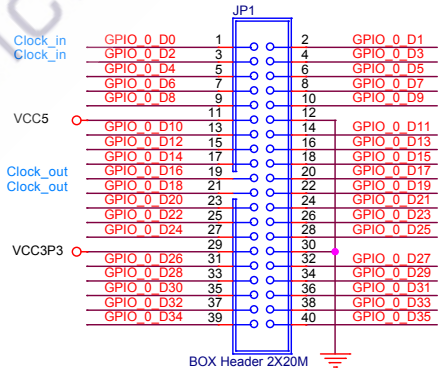


GPIO 0

GPIO_0[35..0] 4,5,6,7



GPIO 0

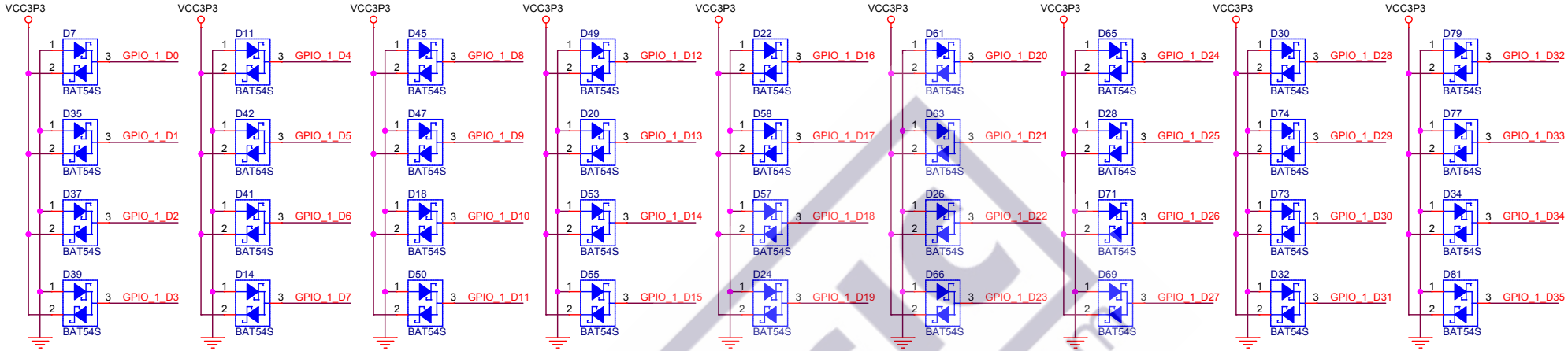


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title
DE0-CV Board

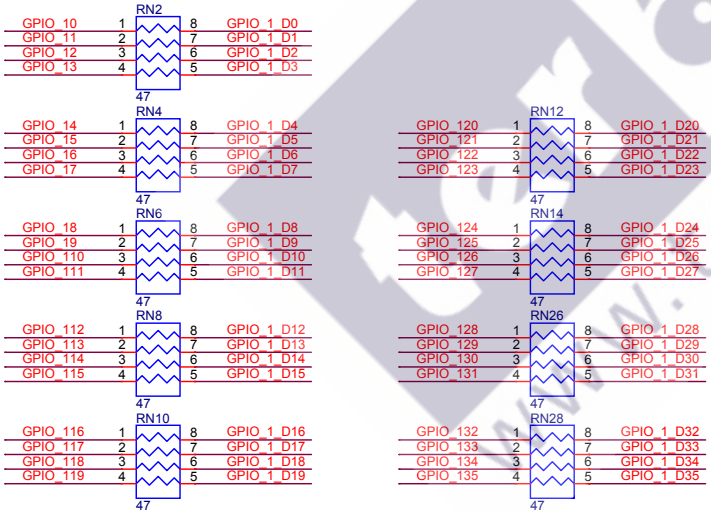
Size	Document Number	Rev
B	GPIO 0	C

Date: Friday, July 03, 2015 Sheet 12 of 17

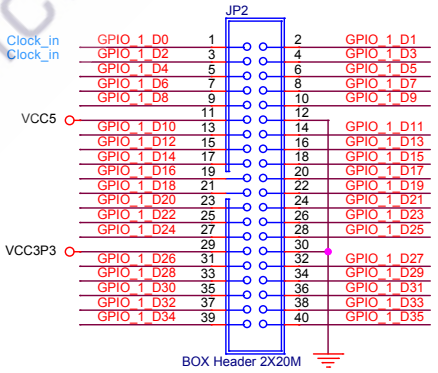


GPIO 1

GPIO_1[35..0] 5,6



GPIO 1

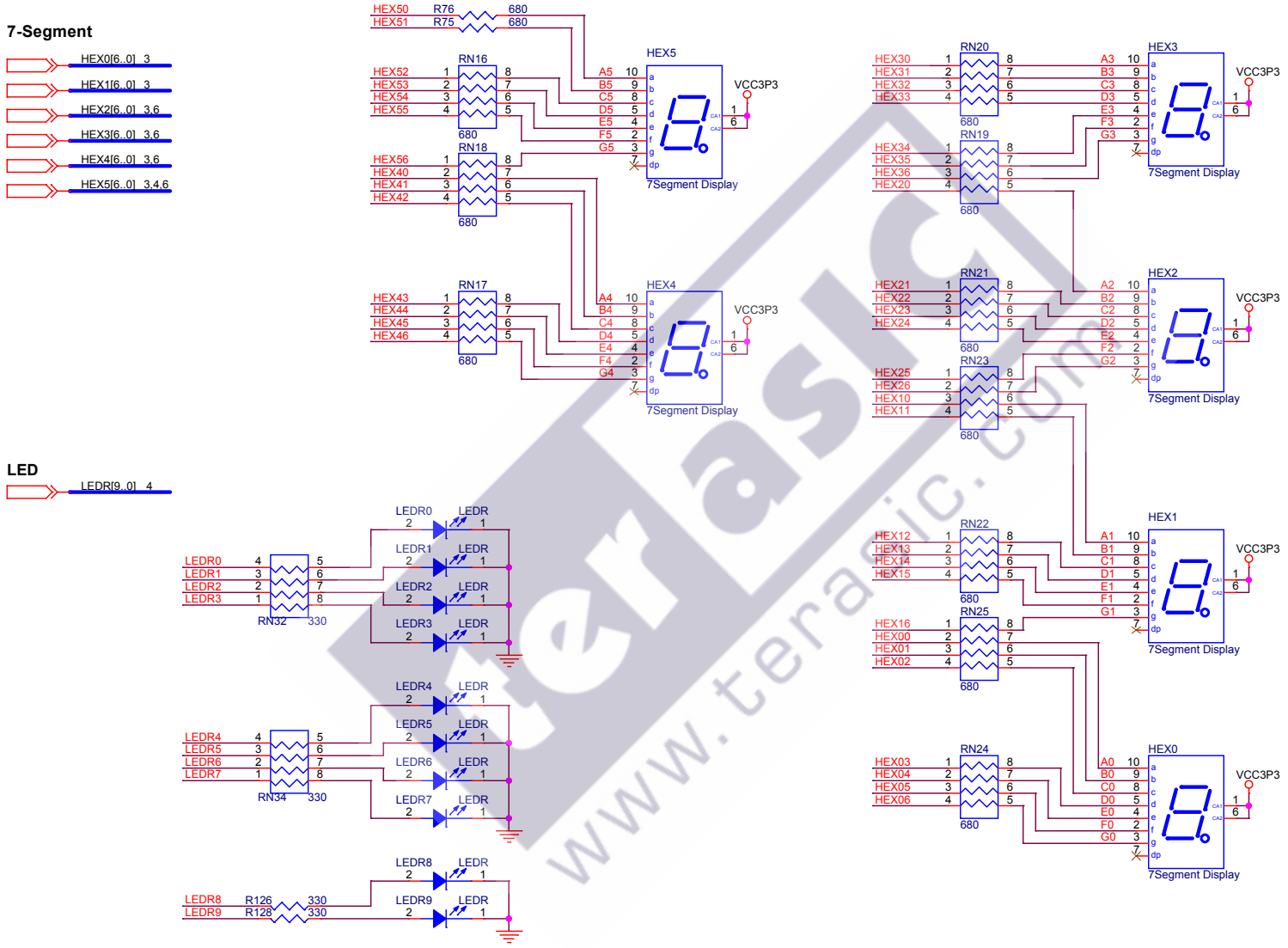


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title
DE0-CV Board

Size	Document Number	Rev
B	GPIO 1	C

Date: Friday, July 03, 2015 Sheet 13 of 17

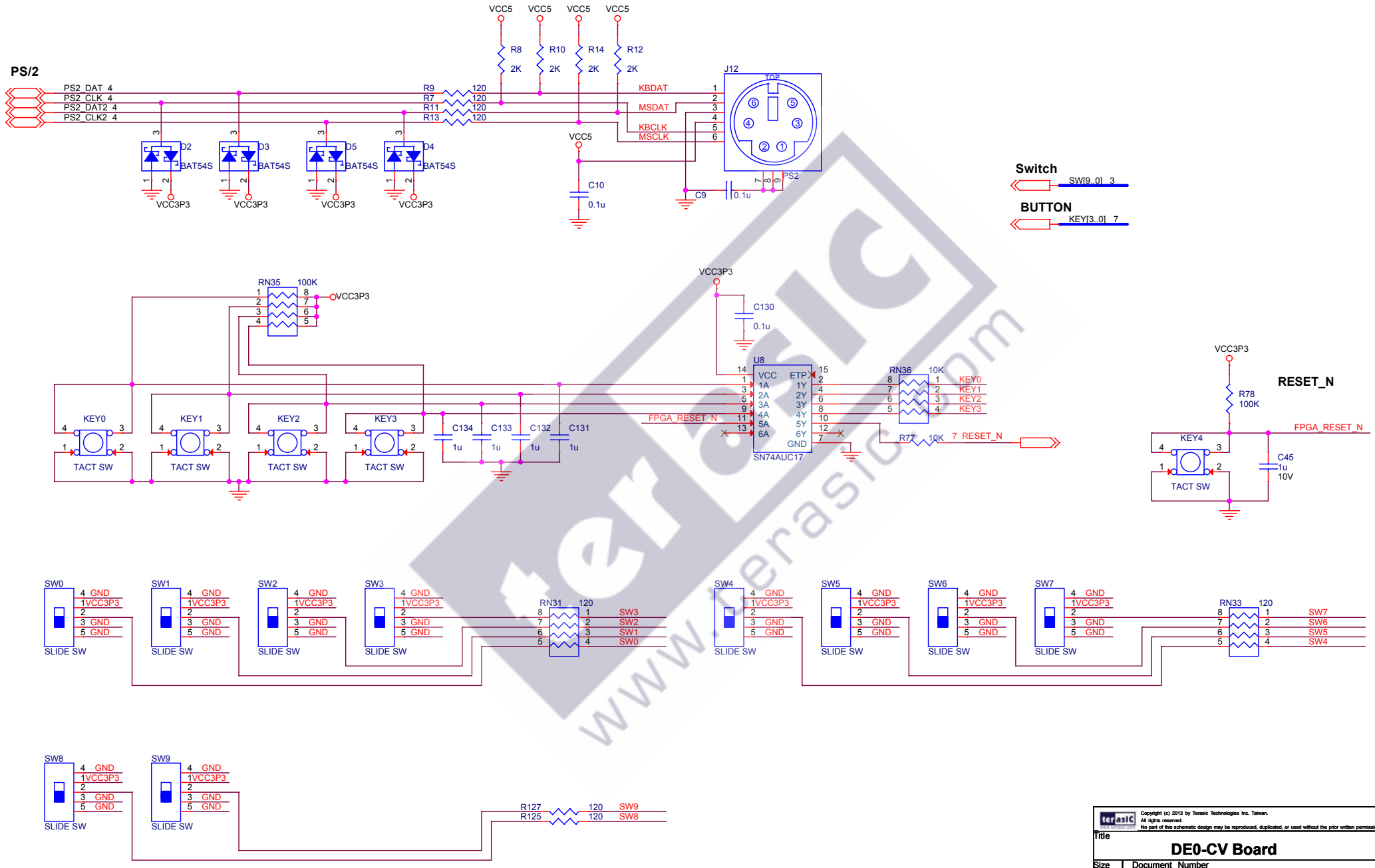


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title
DE0-CV Board

Size	Document Number	Rev
B	7-Segment Display, LED	C

Date: Friday, July 03, 2015 Sheet 14 of 17

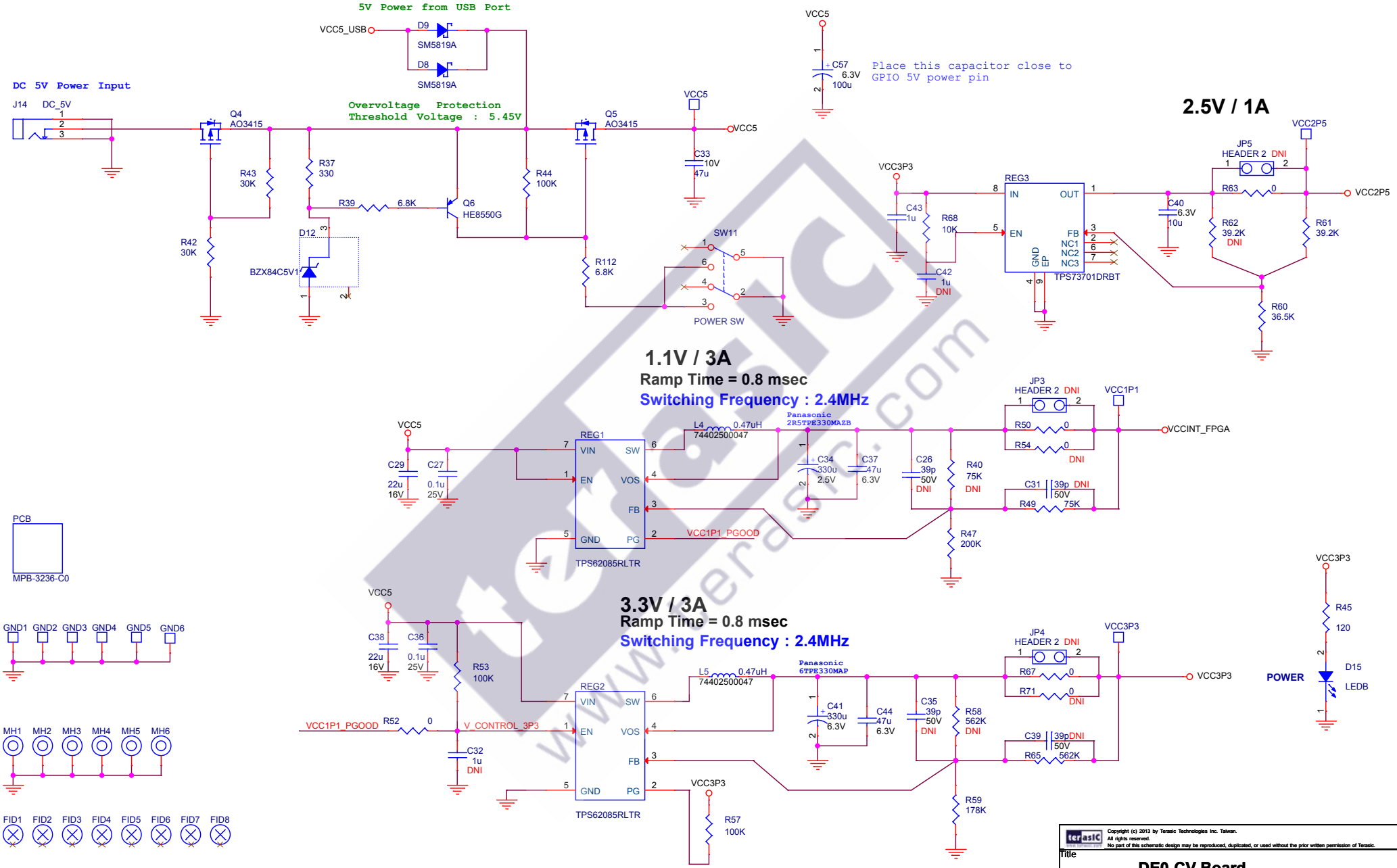


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title
DE0-CV Board

Size	Document Number	Rev
B	PS2, SW , KEY	C

Date: Friday, July 03, 2015 Sheet 15 of 17

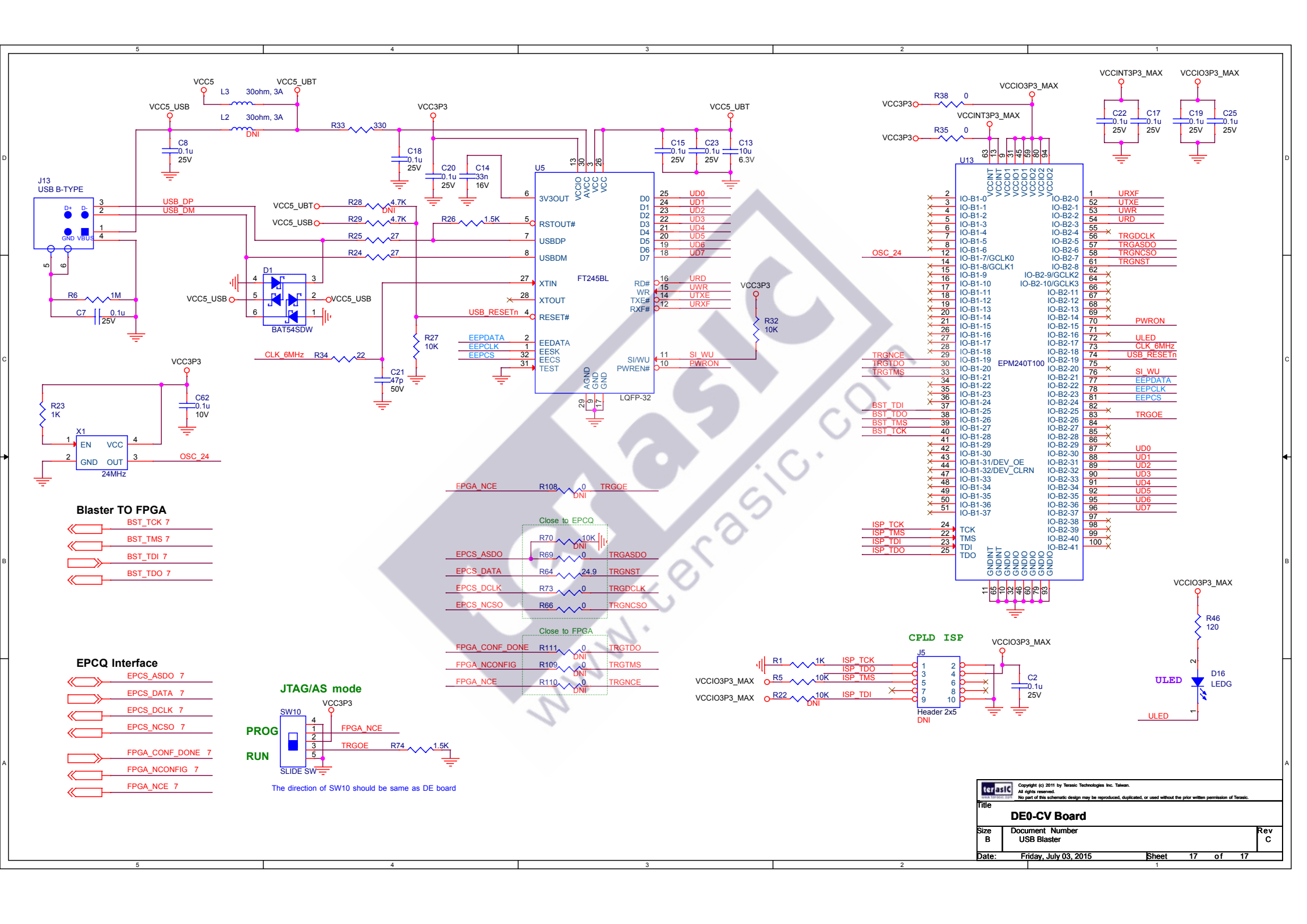


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title
DE0-CV Board

Size	Document Number	Rev
B	Power - 1.1V,2.5V,3.3V,5V	C

Date: Friday, July 03, 2015 Sheet 16 of 17



Copyright (c) 2011 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title: **DE0-CV Board**

Size	Document Number	Rev
B	USB Blaster	C

Date: Friday, July 03, 2015 Sheet 17 of 17